REMARKS

Claims 1-3, 5-15, and 17-29 will be pending upon entry of the present amendment. Claims 1, 9, and 15 are being amended. Claims 4 and 16 are being cancelled. Claims 21-29 are new.

Claim 15 was objected to and claims 15-20 were rejected under 35 U.S.C. § 112, second paragraph for referring to "the second conductive region" in line 10 and "a second conductive region" in line 16. Claim 15 is being amended to refer to "the first conductive region" in line 10. Accordingly, amended claim 15 and dependent claims 17-20 particularly point out and distinctly claim the invention.

The applicant appreciates the indication that claims 4 and 16 were directed to allowable subject matter. Claims 1 and 15 are being amended to include the elements of claims 4 and 16, respectively, which are being cancelled. Thus amended claims 1 and 15 and dependent claims 2-3, 5-8, and 17-20 are in condition for allowance.

Claims 9 and 12 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,854,515 to Bandyopadhyay et al. ("Bandyopadhyay").

Bandyopadhyay does not disclose the invention recited in claims 9 and 12, as amended. Claim 9 is being amended to recite a method of forming an integrated semiconductor structure that includes first and second conductive plugs (39, 57) directly contacting each other and third and fourth conductive plugs (37, 55) that are directly coupled to each other by a second conductive region (40) by forming the first and third plugs simultaneously and the second and fourth simultaneously (the parenthetical references are included for exemplary purposes only and are not intended to limit the scope of the claim to any of the disclosed embodiments). In particular, amended claim 9 recites:

forming a first conductive plug that fills a first opening and is electrically coupled to the first conductive region, the first conductive plug having an upper surface extending no further than the upper surface of the first insulating layer;

forming a second conductive plug that fills the second opening and is electrically coupled to the first conductive plug, the second conductive plug directly contacting the upper

surface of the first conductive plug, and further having an upper surface extending no further than the upper surface of the second insulating layer;

forming a third opening through the first insulating layer;

forming a third conductive plug that fills the third opening and has an upper surface extending no further than the upper surface of the first insulating layer, the first and third conductive plugs being formed simultaneously;

forming a fourth opening through the second insulating layer in a position not directly above the third conductive plug;

forming a fourth conductive plug that fills the fourth opening, second and fourth conductive plugs being formed simultaneously; and

forming a second conductive region over the first insulating layer, the second conductive region directly electrically coupling the third conductive plug to the fourth conductive plug.

Bandyopadhyay does not such steps for forming third and fourth conductive plugs and the second conductive region. Figure 2 of Bandyopadhyay shows a lower portion 20 of a conductor 14b that is formed in addition to upper and lower portions 32, 34 of a conductor 30, but the lower portion 20 is not formed simultaneously with the lower portion 34 and is not connected by a second connecting region to another conductor that is formed simultaneously with the upper portion 32. Accordingly, amended claim 9 and dependent claims 10-14 are not anticipated by Bandyopadhyay.

Claim 9 was also rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,239,491 to Pasch et al. ("Pasch").

Pasch also does not disclose the invention recited in claim 9, as amended. In particular, Pasch does not disclose the claimed steps of forming a fourth conductive simultaneously with forming a second conductive plug and forming a second conductive region that directly couples such a fourth conductive plug to a third conductive plug. Pasch shows in Figure 3 filled vias 152, 154, 157, 158, 160 through a second insulating layer 150, but none of those filled vias is connected to one of the filled vias 132, 134, 136, 138, 140, 142 by a second

conductive region. Further, amended claim 9 recites that the fourth conductive plug fills a fourth opening through the second insulating layer in a position not directly above the third conductive plug. In contrast, all of the filled vias 152, 154, 157, 158, 160 through the second insulating layer 150 are directly above the corresponding filled vias 132, 134, 136, 138, 140, 142 of the first insulating layer 130. Accordingly, amended claim 9 is not anticipated by Pasch.

Claim 10 was rejected under 35 U.S.C. § 103 as being unpatentable over Pasch in view of Wolf.

Pasch and Wolf do not teach or suggest the invention recited in claim 10, which depends on amended claim 9. In particular, Wolf does not teach or suggest the features of claim 9 described above as missing from Pasch. Instead, Wolf deals with ion implanting of dopants without mentioning any conductive plugs or insulating layers. Accordingly, claim 10 is nonobvious in view of Pasch and Wolf.

Claims 11 and 13-14 were rejected under 35 U.S.C. § 103 as being unpatentable over Bandyopadhyay in view of U.S. Patent No. 5,891,799 to Tsui.

Bandyopadhyay and Tsui do not teach or suggest the invention recited in claims 11 and 13-14, which depend on amended claim 9. In particular, Tsui does not teach or suggest the features of claim 9 described above as missing from Bandyopadhyay. That is, Tsui does not teach or suggest the above-quoted steps for forming third and fourth conductive plugs and the second conductive region. In Figure 11, Tsui shows two second level vias 4', but neither of those second level vias 4' is connected by a second conduction region to one of the first level vias 4. Moreover, the second level vias 4' are directly above the first level vias 4, and thus, do not fill a "fourth opening through the second insulating layer in a position not directly above the third conductive plug." Accordingly, claims 11 and 13-14 are nonobvious in view of Bandyopadhyay and Tsui.

New claims 21-25 are not anticipated or rendered obvious by the cited prior art. Claim 21 is directed to a method that includes forming a second conductive layer (41) by forming a conductive layer on the first insulating region 32 and etching the conductive layer to remove all of the conductive layer directly above a first through region (37 or 38) to

simultaneously form the second conductive region in a position not aligned and not in contact with the first through region (the parenthetical references are included for exemplary purposes only and are not intended to limit the scope of the claim to any of the disclosed embodiments). No new matter is being presented.

None of the cited prior art teaches or suggest forming a second conductive region from a conductive layer while etching the portion of the conductive layer above a first through region. Bandyopadhyay, Pasch, and Tsui all form a second insulating layer directly on the first insulating layer immediately after planarizing the first insulating layer, and thus, no second conductive region is formed. U.S. Patent No. 5,773,314 to Jiang forms a conductive region 48b on a first insulating layer 42, but does not remove the conductive region 48a at the same time (See Fig. 3). As discussed at col. 6, lines 60-62, Jiang leaves the conductive region 48a in place during later processing to protect the plug 44, and thus, the removal of the conductive region 48a would damage the Jiang device. Accordingly, claims 21-25 are not anticipated or rendered obvious by the cited prior art.

New claims 26-29 also are not anticipated or rendered obvious by the cited prior art. Claim 26 recites a method that includes forming an etch stop layer (46a) of a first dielectric material on the second conductive region (41) and the first insulating region (32); and forming on the etch stop layer a second insulating region (45a) of a second dielectric material different than the etch stop layer (although the parenthetical references refer to an exemplary embodiment shown in Figure 9, they are not intended to limit the scope of the claim to any of the disclosed embodiments). No new matter is being presented.

None of the cited references teaches or suggests forming an etch stop layer on a second conductive region and below a second insulating region. The Examiner noted with respect to claims 6-7 and 18-19 that U.S. Patent No. 6,165,839 to Lee et al. ("Lee") shows a silicon nitride layer 10 formed on an oxide layer 9. However, the silicon nitride layer 10 is not formed on any second conductive region. Rather, a conductive layer 18b is formed on the silicon nitride layer 10. Accordingly, claims 26-29 are in condition for allowance.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Federico Pio

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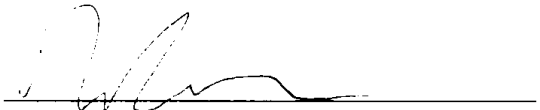

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